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POSZ & BETHARDS, PLC 11250 ROGER BACON DRIVE SUITE 10 RESTON, VA 20190			MONDT, JOHANNES P	
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DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/865,704	Applicant(s) ITO ET AL.	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 and 34-63 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 and 34-63 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 3/21/2003 is: a) ☒ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

Amendment filed 8/22/2003 forms the basis of this office action. Applicant has amended claims 1, 3, 6, 9, 11, 13, 14, 34 and 38 and cancelled claims 29-33. Applicant previously cancelled claims 15-28. Consequently, claims 1-14 and 34-63 are pending in the application (to the original claims Applicant had added new claims 29-63 in an Amendment filed 7/29/2002). Comments on Remarks by Applicant are included below under "Response to Arguments".

Drawings

1. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: the inclusion of a Prior Art Label on Figure 3B. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

Response to Arguments

1. Applicant's arguments filed 8/22/2003 under the heading "Comments and Response" have been fully considered but they are not persuasive.

With regard to comment a) on page 18 (of said Comments and Response):

Acknowledgment of the inclusion of a Prior Art label in Figure 3B has been included above under Drawings and is herewith approved.

With regard to comment b) on said page 18:

Traverse has been accepted in light of the references to the Specification, which may serves as a definition of "inner wall".

With regard to comment c) starting on page 19:

Applicant unfortunately has misunderstood the comments made by the examiner on page 3 of the previous detailed office action (Non-Final Rejection mailed 4/22/03): the examiner stated that if "Applicant would implement a *redefinition* of impurity concentration profile to pertain exclusively to p-type impurities (which so far has not happened, because even when the present definition allows for the statement that said impurity concentration profile results from impurities of a second conductivity type, as well as from impurities of the first conductivity type), then no such gentle peak, or any peak for that matter, can be discerned in Fig. 3B". Although said redefinition helps address the essence of the invention, above cited statement by Applicant could not be construed as a statement of conditional allowance, because said statement is only concerned with a comparison with the prior art Figure 3B. The present claim language is new in a substantial manner and has been searched now at the earliest possible time. As elaborated in the art rejections below, Hshieh et al (5,907,776), in the art of vertical power MOSFET technology (cf. title and abstract), teach a multi-humped impurity concentration profile in the channel-containing region (cf. col. 5, lines 13-47), being inherently multi-peaked because said profile is brought about by a superposition of three individual implantation steps (cf. col. 5, lines 48-61), for the specific purposes of reducing the threshold voltage (cf. col. 5, lines 30-32) and shortening the channel length (cf. col. 5, lines 45-47), which would have been obvious to include in the teaching

of the prior art as admitted by Applicant, at least considering the stated goal of said prior art as admitted by Applicant, a/o to reduce the ON voltage (cf. page 1, line 24 of the Specification). Therefore, regretfully, claims 1-2 again had to be rejected.

With regard to comment d) starting on page 21: the examiner respectfully points out that, *arguendo*, if the trench 34 in Huang would extend “into the substrate or first conductivity layer” as argued by Applicant on page 21, then said trench should be in contact with n-type conductivity material, which is not the case, with reference to Figures 8, 9 and 12-14. Next, concerning Applicant’s allegation that there “is no indication or suggestion in any of the references or specifically Huang et al that the buried layer 35 is two layers”, Applicant is reminded of the nature of an ion implantation step, which is the processing step Huang has used (cf. col. 2, l. 35-38): as shown by S. Wolf (“Silicon Processing for the VLSI Era”, Volume 2 – “Process Integration” (Lattice Press, Sunset Beach, CA, ISBN 0-961672-4-5, published in 1990), particularly pages 658-663 the long penetration tail of the ion implantation concentration profile is a monotonically decreasing function of depth (cf. Equations 9-1 and 9-2, on p. 660, Figures 9-10 (a) and 9-10(b) by a law of nature (experimental profile (a)) confirmed by numerical and analytical-numerical simulations (Fig. 9-10(b)). Rather than a single layer a plural continuum of layers (which inherently contains a plurality of two layers as implied by the claim language), each next one embedding the other, results from a single ion implantation step, such that each next layer is characterized by a concentration lower than the embedded one. Therefore, the recited portion of claim 34 is met by the cited prior art (Huang).

Regarding the traverse of the rejection of claim 38 (page 22 of said Comments and Response), Applicant notes that the “second conductivity type island” “isolated from the second semiconductor layer and being in an electrically floating state” is “beyond the active area for the structure of Huang; however, this does not correspond to any limitation in the claim language, “active area” not being claimed, and none of the claim language otherwise implying that said second conductivity type island must be in said active area. Furthermore, mask 12 in Huang is implemented to protect the polysilicon layer from establishing contact (cf. col. 2, l. 21-27). Said contact can only mean electrical contact because said mask is spaced apart from said polysilicon layer, and hence no material contact could be prevented. Because said “second conductivity type island” is positioned between and abutting both said mask and the same dielectric coating of 26 that is available at the position of the mask any bias imparted on said second conductivity island would be wholly inconsistent with the invention of Huang as expressed with regard to mask 12 and its purpose and location, i.e., col. 2, l. 21-27. As in Applicant’s disclosure, said second conductivity island (portion 14 to the left of first trench 20) is isolated from the second semiconductor layer (portion 14 to the right of first trench 20) by said first trench. Therefore, the rejection of claim 38 is maintained even after the amendment.

Identical or at least essentially identical arguments in traverse of the rejection of claim 51 are not acceptable for the reasons given above in connection with claim 38.

With regard to comments e) on page 23: as noted above, with regard to claim 34, the second trenches shown by Huang do not extend to the substrate but are wholly

embedded in conductivity type material different from that which defines the substrate 10, with reference for the argumentation to the discussion of claim 34. Amended claims 3-5 are now considered for the first time on connection with the prior art found to date.

With regard to comments f), g), and h) starting on page 25, page 26 and page 26, respectively: traverse appears limited to comments given above, apart from reasons that appear rooted in the substantial amendment of the relevant claims.

A final note on the concept of "diffusion region" may have to be added here: doped semiconductor regions in which all or most of the dopants have been introduced through ion implantation may be called diffusion regions, because in addition to the inward momentum with which the ions are implanted said ions perform random motion through their collisions with the constituents of the semiconductor material (atoms or molecules as the case may be). Diffusion is an inherently present phenomenon in the ion implantation process.

Claim Rejections - 35 USC § 102

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. **Claims 34-42 and 51-55** are rejected under 35 U.S.C. 102(e) as being anticipated by Huang (6,110,799). Huang teaches (cf. Figures 9 and 11) a semiconductor device comprising:

- a first semiconductor layer 10 of a first conductivity type (n-type) (cf. column 2, lines 1-2);

- a trench MOS structure formed on the first semiconductor layer (cf. abstract), wherein the trench MOS structure includes:

- a second semiconductor layer 14 of second conductivity type (p-type) located on the first semiconductor layer (cf. column 2, lines 1-5);

- a first trench 20 and 22 as depicted and described in Figure 3 (cf. column 2, lines 14-17) (left-most trench or right-most trench in Figure 9) and corresponding to regions 24 and 26 in Figure 9, penetrating the second semiconductor layer to (reach) the first semiconductor layer;

- a first conductivity type (n-type) doped region 16 (cf. column 2, lines 6-8) located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

- an insulation film 24 (cf. column 2, line 19) covering the semiconductor portion of the trench wall, hence located on what may be called an inner wall of the trench;

- a gate electrode 26 (cf. column 2, lines 18-26) located in the first trench such that the insulation film is located between the inner wall and the gate electrode, hence it may

be said that the insulation film is located between the inner wall surface and the gate electrode;

a second trench 34 (cf. column 2, lines 38-43; cf. Figure 11, where said portion is indicated by the numeral 36) extending into but not through the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region 35 (cf. column 2, lines 38-43) having a junction depth greater than the junction depth of the second semiconductor layer by virtue of its protrusion downward from said second semiconductor layer, the protrusion being positioned beneath the second trench 34; while because of the method of making of said second conductivity type protrusion region 35, i.e., ion implantation (cf. column 2, lines 34-37), region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

Finally, Huang also teaches an upper electrode of metal 36 contacting the first conductivity type doped region of the trench MOS structure through the second trench. Therefore, Huang anticipates claim 34.

With regard to claim 37: the semiconductor device of claim 34 as taught by Huang has the property that the junction depth D1 of the second conductivity type protrusion region 34 is greater than the depth of the first trench (cf. column 3, lines 1-4).

With regard to claim 38: Huang teaches (Figure 9) a semiconductor device comprising:

- a first semiconductor layer 10 of first conductivity type (n-type) (cf. column 2, lines 1-2);

- a trench MOS structure formed on the first semiconductor layer (cf. abstract), comprising:

- a second semiconductor layer consisting of the regions 14 to the right of the left-most first trench in Figure 9, of second conductivity type (p-type) (cf. column 2, lines 1-5);

- a first trench (indicated as 20 and 22 on Figure 3 (cf. column 2, line 11) and comprising regions 24 and 26 in Figure 9; see column 2, lines 18-21) penetrating the second semiconductor layer to (reach) the first semiconductor layer;
 - a first conductivity type doped region 16 (n-type) (cf. column 2, lines 5-8) located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

- an insulation film 24 (cf. column 2, lines 14-17) located on the interface between the trench and the first and second semiconductor layers;

a gate electrode 26 (cf. column 2, lines 18-26) located in the first trench such that the insulation film both abuts and separates the trench wall and the gate electrode;

a second conductivity type island 14 to the left of the left-most first trench in Figure 9, i.e., located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer by said first trench.

Furthermore, said second conductivity type island is being held in a floating state because mask 12 in Huang is implemented to protect the polysilicon layer from establishing contact (cf. col. 2, l. 21-27). Said contact can only mean electrical contact because said mask is spaced apart from said polysilicon layer, and hence no material contact could be prevented. Because said "second conductivity type island" is positioned between and abutting both said mask and the same dielectric coating of 26 that is available at the position of the mask any bias imparted on said second conductivity island would be wholly inconsistent with the invention of Huang as expressed with regard to mask 12 and its purpose and location, i.e., col. 2, l. 21-27;

an upper electrode 36 (cf. column 2, lines 38-43), which contacts the first conductivity type doped region 35 of the trench MOS structure through a second trench 34 (cf. column 2, lines 38-43 and Figure 8), wherein the upper electrode is isolated from said second conductivity type island to the left of the left-most first trench.

With regard to claim 39: the trench MOS structure in the semiconductor device according to claim 38 as taught by Huang further comprises a second conductivity protrusion region 35 (cf. column 2, lines 38-43), the junction depth of which is greater

than the junction depth of the second semiconductor layer (cf. column 3, lines 1-5), and wherein the protrusion region is positioned away from the first trench.

With regard to claim 40: the trench MOS structure of the semiconductor device according to claim 39 as taught by Huang further comprises a second trench 34 (cf. column 2, lines 38-43) located in the second conductivity type region and positioned away from the first trench, the protrusion region 35 being positioned beneath the second trench (see Figure 9).

With regard to claim 41: Because region 35 as taught by Huang is formed by ion implantation (cf. column 2, lines 34-37) region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a diffusion depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

With regard to claim 42: the junction depth of the second conductivity type protrusion region 35 in the semiconductor device of claim 39 as taught by Huang is greater than the depth of the first trench (cf. column 3, lines 1-5).

With regard to claim 51: Huang teaches (cf. Figure 9) a semiconductor device comprising:

a first semiconductor layer of first conductivity type (n-type) (cf. column 2, lines 1-2);

a second semiconductor layer 14 of second conductivity type (p-type) located on the first semiconductor layer (cf. column 2, lines 1-5);

a first trench (the one most to the left in Figure 9 and indicated by numerals 20, 22 in Figure 3 and 24/26 in Figure 9) penetrating the second semiconductor layer to (reach) the first semiconductor layer, wherein the second semiconductor layer is divided into a first portion (to the right of said first trench) and a second portion (to the left of said first trench), the second portion being isolated from the second portion by means of insulation film 24 (cf. column 2, line 15); a first doped region 16 (cf. column 2, lines 6-8) of first conductivity type inside the first portion of 14 and proximate to the opening of the first trench (namely that part of 16 that is to the right of said first trench); a second doped region 16 (cf. column 2, lines 6-8) of first conductivity type located inside the second portion of 14 and proximate to the opening of the first trench (namely that portion of 16 that is to the left of said first trench); an insulation film 24 (cf. column 2, line 15) on an inner wall of the first trench; a gate electrode 26 (cf. column 2, lines 18-26) located in the first trench, wherein a first trench MOS structure is collectively formed with the first semiconductor layer, the first portion and first doped region, and a second trench MOS structure is collectively formed with the first semiconductor layer, the second portion and the second doped region, the material constitution being that of a

UMOS structure, in which said first and second doped regions constitute the sources and the first semiconductor layer constitutes the drain, and with the first and second portions of 14 constituting the body regions of said UMOs structure; and an upper electrode 36 (cf. column 2, lines 38-43) contacting the first doped region 16 and first portion 14 of the first trench MOS structure, wherein the second doped region and the second portion of the second trench MOS structure, i.e., the one most to the left, are in an electrically floating state by virtue of the total electrical isolation of said second doped region and said second portion both polysilicon gate and metal electrodes 26 and 36, respectively.

With regard to claim 52: the trench MOS structure in the semiconductor device according to claim 51 as taught by Huang further comprises a second conductivity protrusion region 35 (cf. column 2, lines 38-43), the junction depth of which is greater than the junction depth of the second semiconductor layer (cf. column 3, lines 1-5), and wherein the protrusion region is positioned away from the first trench.

With regard to claim 53: the trench MOS structure of the semiconductor device according to claim 52 as taught by Huang further comprises a second trench 34 (cf. column 2, lines 38-43) located in the second conductivity type region and positioned away from the first trench, the protrusion region 35 being positioned beneath the second trench (see Figure 9).

With regard to claim 54: Because region 35 as taught by Huang is formed by ion implantation (cf. column 2, lines 34-37) region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the

location as measured by its distance to the trench. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a diffusion depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

With regard to claim 55: the junction depth of the second conductivity type protrusion region 35 in the semiconductor device of claim 52 as taught by Huang is greater than the depth of the first trench (cf. column 3, lines 1-5).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. ***Claims 1-2*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted in Applicant's disclosure in view of Hshieh et al (5,907,776).

With regard to claim 1: Prior Art, for instance as explicitly admitted by Applicants in their disclosure (cf. page 2 of Specification and Fig. 22B), teaches:

a semiconductor substrate 12/12a (cf. page 2, lines 12-13) having a first conductivity type (n-type) layer 12 at a principal surface and a second conductivity type layer 12a (p-type) at a rear surface;

a second conductivity type (p-type) diffusion region 3 having island shape (cf. page 2, line 17), formed on the principal surface of said semiconductor substrate wherein the second conductivity type diffusion region has an impurity concentration profile resulting from impurities of a second conductive type in a depth direction of the semiconductor substrate (see Figure 3B; cf. also page 21 lines 9-10 of the disclosure);

a highly doped first conductivity type region 4 (cf. page 2, lines 21-22) inside said second conductivity type diffusion region, wherein said impurity concentration profile of said second conductivity type impurity has a gentle peak (cf. Figure 21, said gentle peak indicated with downwardly pointing arrow above the p-body region) (i.e., "gentle" meaning: well represented by a continuously differential function) at a depth that is greater than a junction depth of said first conductivity type diffusion region (junction with said second conductivity type diffusion region);

a trench 5 (cf. page 2, line 22) formed in the semiconductor substrate extending from a surface of said first conductivity type diffusion region through said second conductivity type region 3 to said first conductivity type layer 12 on said semiconductor substrate (cf. Fig. 22B);

an insulation film 6 (cf. page 2, line 24) formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon 7 (forming the gate electrode 8) (cf. page 2, line 26 – page 3, line 2) filling said trench with said insulation film interposed there between (cf. Fig. 22B).

Prior Art as admitted by Applicant does not necessarily teach the further limitation that said impurity concentration profile of said second conductivity type impurity has a plurality of peaks at different depths, rather than just a single peak at a certain depth. However, it would have been obvious to include said further limitation in view of Hshieh et al, who, in the art of vertical power MOSFET technology (cf. title and abstract), teach a multi-peaked impurity concentration profile in the channel-containing region (cf. col. 5, lines 13-47), being inherently multi-peaked because said profile is brought about by a superposition of three individual implantation steps (cf. col. 5, lines 48-61), each introducing a peak in the distribution of impurities, for the specific purposes of reducing the threshold voltage (cf. col. 5, lines 30-32) and shortening the channel length (cf. col. 5, lines 45-47), which would have been obvious to include in the teaching of the prior art as admitted by Applicant, at least considering the stated goal of said prior art as admitted by Applicant, a/o to reduce the ON voltage (cf. page 1, line 24 of the Specification).

Motivation to include the teaching by Hshieh et al into the Prior Art as admitted by Applicant thus stems from the common purpose in fully analogous

art to reduce the threshold voltage in trench-type. Combination of said teaching with the invention in the Prior Art as admitted by Applicant is straightforward through implementing superposed ion implantation steps following Hshieh et al in applying standard technology in this regard.

With regard to claim 2: the electrode portion of claim 1 as taught by the Prior Art as disclosed by Applicants in Fig. 22B is formed to have a T-shaped cross section composed of a first part filling the trench and the second part protruding on the principal surface of the semiconductor substrate (cf. Fig. 22B, particularly the T shape of the region with numeral 8).

2. ***Claims 3 – 5 are rejected*** under 35 U.S.C. 103(a) as being unpatentable over the Prior Art as disclosed by Applicants (cf. pages 2-3 of the Specification) in view of Huang (6,110,799).

Prior Art, for instance as explicitly admitted by Applicants in their disclosure (cf. page 2 of Specification and Fig. 22B), teaches:

a semiconductor substrate 1 (cf. page 2, lines 12-13) having first conductivity type layer 12 at a principal surface and a second conductivity type layer 12a at a rear surface;

a second conductivity type diffusion region 3 formed on the principal surface of said semiconductor substrate having island shape (cf. page 2, line 17);

a highly doped first conductivity type region 4 (cf. page 2, lines 21-22) formed inside said second conductivity type diffusion region, said first

conductivity type inherently due to the introduction of impurities of the first conductivity type at high concentration;

a plurality of trenches or first trenches 5 (cf. page 2, line 22) each extending from a surface of said highly doped first conductivity type region said second conductivity type diffusion region to said first conductivity layer of said semiconductor substrate (cf. Fig. 22B), thereby defining a channel portion on a wall surface of each of said first trenches;

an insulation film 6 (cf. page 2, line 24) formed on an inner wall surface of each of the first trenches; and

an electrode portion made of polycrystalline silicon 7 (forming the gate electrode 8) (cf. page 2, line 26 – page 3, line 2) filled in each of the first trenches with said insulation film interposed there between (cf. Fig. 22B).

The Prior Art as disclosed by Applicants does not necessarily teach a plurality of second trenches and a second conductivity type protrusion region as stipulated in Applicants' claim 3.

However, for the specific purpose of protecting the gate trenches against breakdown, Huang (cf. Fig. 9) teaches a semiconductor device with trenches (cf. abstract, first sentence) comprising a plurality of first trenches with an electrode portion 26 made of polysilicon (cf. column 2, line 24) and insulation layer 24 (cf. column 2, line 15) similar to Applicants' first trenches, and also comprising a plurality of second trenches 34 (cf. Fig. 8 and column 3, line 39; see also column 2, lines 32 and 42) (the plurality of which is implied by the function of said second trenches as structures to be placed in between

adjacent members of the said plurality of first trenches, said latter plurality being inclusive of the possibility of more than two first trenches) formed to extend into but not through said second conductivity type region 14 (cf. column 2, line 5) so that each of the second trenches is positioned between an adjacent pair of said first trenches in parallel with said first trenches (cf. Fig. 11), such that a second conductivity type (P type) protrusion region 35 (cf. Fig. 9 and column 2, lines 41-42) is formed with a junction deeper than the junction of said second conductivity type region (cf. column 3, lines 1-4) and in electrical contact with the highly doped first conductivity type region 14. It is inherent in impurities in semiconductor material that they must have been introduced while, because of the election by Applicants of the device invention, as opposed to a method of making invention, the manner in which said impurities may be introduced is irrelevant to the present examination of the invention. Said protrusion region protrudes downwardly forming a junction that is deeper than a junction of said second conductivity type region (cf. column 3, lines 1-5), the protrusion being positioned beneath the second trench. *The aforementioned purpose for including the second trenches and protrusion, namely the protection against breakdown of the trench gates, is obviously useful in the specific case of the plurality of first trenches admitted to be prior art by Applicants.*

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as taught by the prior art as admitted by Applicants at the time it was made so as to include the further limitations involving the definitions of said plurality of second trenches and said second conductivity type protrusion region.

Finally, because the protrusion region 35 is formed by ion implantation (cf. column 2, lines 34-37) region 35 is by necessity characterized by a monotonically decreasing impurity concentration as a function of the depth of the location as measured by its distance to the trench and resulting in a plural continuum of layers (which inherently contains a plurality of two layers as implied by the claim language), each next one embedding the other, results from a single ion implantation step, such that each next layer is characterized by a concentration lower than the embedded one. Region 35 can thus be divided into two abutting sub-regions that together form region 35, such that one region, henceforth called a "second conductivity type highly doped region" has an impurity concentration higher than that of the remaining region (henceforth called "protrusion region") and has a depth less than that of the junction of the protrusion region, the second conductivity type highly doped region being located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

With regard to claim 4: the Prior Art as admitted by Applicants teaches the said electrode portion to have a T shaped cross section composed of a first part filling the trench and a second part protruding on the principal surface of the substrate (cf. Fig. 22B). Therefore, claim 4 does not distinguish over the prior art.

With regard to claim 5: although the Prior Art as admitted by Applicants do not necessarily teach the further limitation as defined by claim 5, Huang teaches an electrode 36 (cf. column 2, lines 39-43) connecting said highly doped first conductivity type region 16 (cf. Fig. 9) to said second conductivity type protrusion region 35 through

said second trench, said contact being essential in aforementioned protection function of the plurality of second trenches, as explained above in the discussion of claim 3.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 3 at the time it was made so as to include the further limitation of claim 5.

3. ***Claims 6 – 10 are rejected*** under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicants and over Huang as applied to claim 3 above, and further in view of Yu et al (6,213,869 B1). As detailed above, claim 3 is unpatentable over Prior Art as admitted by Applicants in view of Huang.

Although neither the Prior Art as admitted by Applicants nor Huang teach the further limitation as defined by claim 6, it is known in the art as witnessed by Yu et al (cf. abstract, second sentence, and column 1, lines 7-15) that a floating body region creates a capacitor between body region and gate in MOSFET devices, resulting in a higher threshold voltage when the MOSFET is OFF than when it is ON, thus reducing steady state power dissipation. To combine this feature with the trench power MOSFET casu quo IGBT of Applicants is *obvious* because the higher withstand voltage aimed at needs to be achieved at reasonable costs with regard to power dissipation in the ON state. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claim 3 at the time it was made so as to include the further limitation of claim 6.

With regard to claim 7: Huang teaches a first electrode provided in one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity region through one of the second trenches, while the plural nature of said second trenches is implied by their positioning in between the first trenches given the plural nature of said first trenches, comprising the case of more than two; hence Huang also teaches a second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the other one of said second trenches, the second electrode being disposed adjacent to the first electrode.

Although neither Prior Art as disclosed by Applicants nor Huang necessarily teach one of said adjacent pair of first and second electrodes to be in a floating state, said floating state would add the said type conductivity protrusion region to the floating body region for the well-defined *purpose* of enhancing the effect of the capacitor formed between the gate and the thus extended body region, thereby adding to the difference between the threshold voltages in the OFF, respectively ON states, and thus further improving the possibility to combine high OFF state threshold voltage with low power dissipation in the steady state operating mode of the device.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention defined by claim 3 at the time it was made so as to include the further limitation of claim 7.

With regard to claim 8: the second conductivity type protrusion region 35 is itself a highly doped region, and therefore can be thought of as split into two sub-regions, a first part, consisting of a highly doped region contacting said electrode 36 and disposed between said electrode and the remaining (second) part of said second type protrusion region 35. Therefore, the further limitation of claim 8 does not distinguish over the prior art.

With regard to claim 9: in the Prior Art as admitted by Applicants (at least) one of said plurality of first trenches encloses the second conductivity type region diffusion entirely (cf. Fig. 22B). Therefore, the further limitation as defined by claim 9 does not distinguish over the prior art.

With regard to claim 10: Huang teaches the first trenches to be shallower than the second conductivity type protrusion regions (cf. column 3, lines 1-4) for the purpose of trench gate protection. Since each trench gate needs protection it would have been obvious to teach the further limitation of claim 10.

4. **Claims 11 – 14 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicants in their disclosure (pages 2-3 and Fig. 22B) in view of So et al (5,895,951). As detailed above, Prior Art as admitted by Applicants anticipates claim 1.

Said Prior Art does not necessarily teach the further limitation as it is defined by claim 11.

However, the inclusion of a plurality of electric field alleviating regions formed by introducing impurities of the second conductivity type formed in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region has long been known in the art of trench MOSFET structures, as evidenced by So et al, who teach deep-P regions 116 (cf. column 4, line 9-11, and Fig. 2) annex doping trenches 112 *for the specific purpose* of suppressing incidental turn-on of parasitic bipolar transistor function (cf. column 3, lines 33-42). Said regions 116 surround the body region, enclosing a peripheral portion of it. Moreover, said regions are composed of a strip-wise third trench 112 (cf. column 4, line 4) and second conductivity type deep-P regions 116 in which impurities of the second conductivity type have been introduced in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region, whilst the pn junction of the electric field alleviating regions is deeper than a pn junction of aforementioned second conductivity type region (cf. column 3, lines 33-50 and Fig. 2). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by claims 11 – 13.

With regard to claim 14: the further limitation as defined by claim 14 does not add anything to the device specifications and is merely a statement of obvious use. Vertical trench MOSFET devices such as defined by claim 11 have long been known by people of ordinary skills to be useful as gate driving power elements for controlling the conduction state between the back surface of their semiconductor substrate and their source (first conductivity type region in the present invention and claims, usually highly doped, as is the case here (n+)) by using said electrode portion (comprising gate) as a

control electrode. Therefore, the further limitation of claim 14 is moot as device limitation, and does not distinguish Applicants' invention over the prior art.

5. **Claims 35-36, 43-50, and 56-63** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (6,110,799) in view of Prior Art as Admitted by Applicant. As detailed above, Huang anticipates claims 34, 38 and 51.

Huang does not necessarily teach the further limitations of claims 35-36, 43-50 and 56-63. However, it is understood in the art of vertical MOS devices that the drain electrode, inherently present in such devices, is a lower electrode contacting a semiconductor layer on the lower main face of the semiconductor wafer, said semiconductor layer being more highly doped and of a conductivity type that may be opposite to that of the semiconductor material with which it is in contact. See, for instance, Prior Art as Admitted by Applicant, particularly Figure 22B, in which a third semiconductor layer 12a of second conductivity type is located on a rear surface of the first semiconductor layer 12, opposite to the second conductivity layer 13 (claims 35, 43, 45, 47, 49, 56, 58, 60 and 62), while the semiconductor device further comprises a lower electrode contacting said third semiconductor layer (claims 36, 44, 46, 48, 50, 57, 59, 61, and 63). The lower (drain) electrode is an inherent aspect of a UMOS as taught by Huang (cf. abstract), while it is understood in the art of vertical MOSFET technology that the third semiconductor layer serves to form a more highly conductive layer, smoothening the transition with the metallic-like electrode while providing a Zener diode for protection, whence the motivation to include the teaching in this regard by the Prior

Art as Admitted by Applicant in the invention by Huang. The inventions can be combined readily, as nothing in Huang interferes with the provision of said third semiconductor layer and lower electrode. Success of the implementation of the combination of the inventions can therefore be reasonably expected.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

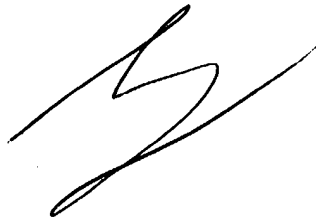
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink, consisting of a stylized, cursive 'J' followed by a series of loops and a long horizontal stroke extending to the right.

JPM
November 4, 2003